SIGNAL-ADJUSTED LCD CONTROL UNIT

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a signal-adjusted LCD control unit and, more particularly, to an LCD control unit in an LCD device which is capable of being adjusted by software to conform to the γ-profile of the LCD panel in the LCD device.

(b) Description of the Related Art

Liquid crystal display (LCD) devices are increasingly used as display devices in a portable electronic equipment including a computer system, such as a mobile telephone. Among other LCD devices, the LCD device used in the mobile telephone is especially requested to have smaller dimensions and smaller weight.

Fig. 1 shows a conventional LCD device, which includes an LCD panel 60, an LCD driver 40 and an LCD controller 70. The LCD driver 40 is formed as a one-chip IC, mounted on the LCD panel 60 for driving the LCD panel 60. The LCD controller 70 is disposed separately from the LCD panel 60 and the LCD driver 40. The LCD controller 70 includes a γ-correction resistor string 71, an impedance converter 72, a voltage divider 73 and a Vcom-voltage generator 74.

Both the γ-correction resistor string 71 and the voltage

divider 73 are connected between a high-voltage source line V_{CC} and a low-voltage source line V_{SS} to generate a plurality (n) of voltages and a plurality (m) of voltages, respectively. The impedance converter 72 converts the impedance of the plurality of voltages supplied from the taps of the γ-correction resistor string 71 to output a plurality of γ-correction voltages 103, which are fed to the LCD driver 40. Each signal line transferring one of the γ-correction voltages 103 is provided with a smoothing capacitor or bypass capacitor (not shown). The LCD driver 40 generates display voltage signals 108 based on the data signal 107 supplied outside from the LCD device and the γ-correction voltages 103, delivering the display data signal 108 to the data electrodes of the LCD panel 60.

The Vcom-voltage generator 74 generates a plurality of Vcom voltages 104 based on the voltages supplied from the voltage divider 73, the Vcom voltages 104 being supplied to the common electrode of the LCD panel 60. The LCD panel 60 is thus driven by the display data signals 108 and the Vcom voltages 104 based on an AC driving scheme to display on the screen thereof images including characters and pictures.

In the conventional LCD device as described above, the LCD driver 40 and the LCD controller 70 have different functions, and are generally disposed outside the LCD panel 60 separately from one another.

It is known that the LC layer of the LCD panel 60 exhibits a

non-linearity of optical transmittance with respect to the display voltage signal applied therethrough. In view of this fact, the LCD driver 40 supplies specific display data signals 108, which are corrected based on the γ-correction voltages corresponding to the γ-profile of the optical transmittance of the LC layer, thereby effecting a suitable contrast on the screen of the LCD panel 60.

Otherwise, if a DC voltage is applied to the LC layer, an electro-chemical reaction arises on the surface of the electrodes of the LCD panel, whereby the lifetime of the LCD panel 60 will be significantly reduced. The AC driving scheme is such that the polarity of the drive voltage between the data electrodes and the common electrode is reversed at a constant cycle. The applied AC voltage, however, are often subjected to deformation of the waveform to cause an inequality in the waveform between the positive-polarity duration and the negative-polarity duration of the applied voltage. The inequality of the waveform in fact generates some DC component of the applied voltage signal, thereby causing an undesirable phenomenon such as flickering of the screen. The Vcom voltages as described above cancel the inequality of the waveform by changing the voltage level of the common electrode between both the durations, to thereby suppress the adverse effect by the DC component.

The γ-correction voltages and the Vcom voltages respectively have suitable values corresponding to the inherent characteristics of the respective LCD panels. This necessitates an

initial adjustment of the γ-correction voltages and the Vcom voltages before the LCD panel is installed in service. The initial adjustment is generally conducted by a hardware work which determines the resistances of resistors of the γ-correction resistor string 71 and the voltage divider 73 provided as external resistors. In particular, the resolution of the γ-voltages generated by the γ-correction resistor string 71 is reduced after the adjustment by the external resistors, which necessitates incorporation of additional resistors to cancel the reduction of the resolution and thus complicates the work for the hardware adjustment.

In addition, the hardware adjustment of the LCD device especially increases the costs and the dimensions thereof due to the complicated structure of the LCD device including the LCD panel 60, LCD driver 40, the LCD controller 70 and the external members associated therewith.

SUMMARY OF THE INVENTION

In view of the above problems in the conventional LCD device, it is an object of the present invention to provide an LCD control unit for use in an LCD device, which is capable of being adjusted by a signal such as a software and thus reducing the dimensions and costs of the LCD device.

The present invention provides an LCD control unit for driving an LCD panel in an LCD device, said LCD control unit comprising:

a signal controller for generating a voltage address signal and a polarity control signal;

a voltage generator block for generating a plurality of (n) γ -voltage levels and a plurality of (m) Vcom-voltage levels based on said voltage address signal,

a voltage selecting block for selecting a specified number of said γ -voltage levels and one of said Vcom-voltage levels based on said polarity control signal to output said specified number of γ -correction voltages and a Vcom voltage; and

an LCD driver for generating a set of display data signals based on a set of external data signals, said LCD driver including a γ -correction section for correcting voltages of said display data signals based on said specified number of γ -correction voltages.

In accordance with the LCD control unit of the present invention, since the γ -correction voltages can be corrected based on the specified number of γ -voltage levels, adjustment for the γ -correction voltages can be effected by software work, without including a hardware work.

The above and other objects, features and advantages of the present invention will be more apparent from the following description, referring to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a conventional LCD device.

Fig. 2 is a block diagram of an LCD device including an LCD control unit according to an embodiment of the present invention.

Fig. 3 is a block diagram of the voltage generator block shown in Fig. 2.

Fig. 4 is a block diagram of the impedance converter shown in Fig. 2.

Fig. 5 is a block diagram of the LCD driver shown in Fig. 2.

PREFERRED EMBODIMENTS OF THE INVENTION

Now, the present invention is more specifically described with reference to accompanying drawings, wherein similar constituent elements are designated by similar reference numerals throughout the drawings.

Referring to Fig. 2, an LCD device includes an LCD panel 60 and an LCD control unit 10 according to an embodiment of the present invention. The LCD control unit 10 includes a signal controller (or software adjustment block) 50 for generating a voltage address signal 105 and a polarity control signal 106, a voltage generator block 20 for generating a plurality of (n) γ-voltages 101 and a plurality of (m) Vcom voltages 102 based on the voltage address signals 105, an impedance converter (or voltage selecting block) 30 for converting the impedances of the γ-voltages 101 and the Vcom voltages 102 and selecting some of the γ-correction voltages 103 and the Vcom-voltage signals 104

based on the polarity control signal 106, and an LCD driver 40 for generating display voltage signals 108 based on the data signals 107 supplied from outside the LCD device and the γ-correction voltages 103. The Vcom-voltage signals 104 are supplied to the LCD panel 60 for driving the LCD panel 60 in an AC driving scheme while canceling the DC component of the display data signals 108.

The LCD control unit 10 is manufactured as a one-chip IC mounted on the LCD panel 60. The configuration of the LCD control unit 10 significantly reduces the dimensions and weight of the LCD device.

The signal controller 50 supplies the voltage address signal 105 to the voltage generator block 20, and the polarity control signal 106 to the impedance converter 30. The voltage generator block 20 generates n γ-voltages 101 and m Vcom voltages 102 based on the voltage address signal 105, and delivers the γ-voltages 101 and the Vcom voltages 102 to the impedance converter 30.

The impedance converter 30 converts the internal impedances of the γ-voltages 101 and the Vcom voltages 102 to generate γ-correction signals 103 and Vcom-voltage signals 104, which are delivered to the LCD driver 40 and the LCD panel 60, respectively. The LCD driver 40 converts the data signal 107 to the display data signals 108 by using the γ-correction voltages, and delivers the display data signals 108 d to the LCD panel 60.

Referring to Fig. 3, the voltage generator block 20 includes an adjustment resistor string 21, a γ-voltage generator block 22 and a Vcom-voltage generator block 23. The adjustment resistor string 21 includes a plurality of (X+1) resistors R_{a1}-R_{ax+1} connected in series between a high-potential source line V_{CC} and a low-potential source line V_{SS}.

The resistors R_{a1}-R_{ax+1} have the resistances substantially equal to one another, and equally divide the voltage between the high-potential source line V_{CC} and the low-potential source line V_{SS} to generate X voltage levels Va(1)-Va(X), which are delivered to the γ-voltage generator block 22 and some of which are delivered to the Vcom-voltage generator block 23.

The γ-voltage generator block 22 includes n data latches 20_1-20_n, n decoders 21_1-21_n, and n multiplexers 22_1-22_n. For example, n is four. Data latch 20_1, decoder 21_1, and multiplexer 22_1 constitute a first γ-voltage generator section, whereas data latch 20_n, decoder 21_n and multiplexer 22_n constitute n-th γ-voltage generator section.

The Vcom-voltage generator block 23 includes m data latches 23_1-23_m, m decoders 24_1-24_m, and m multiplexers 25_1-25_m. Data latch 23_1, decoder 24_1 and multiplexer 25_1 constitute a first Vcom-voltage generator section, whereas data latch 23_m, decoder 24_m and multiplexer 25_m constitute a m-th Vcom-voltage generator section.

The adjustment resistor string 21 generates X (=n $\times$ L)

voltage levels at respective taps thereof, and delivers voltage levels Va(1)-Va(L) to multiplexer 22_1, voltage levels Va(L+1)-Va(2L) to multiplexer 22_2, $\cdots$, and voltages levels Va((n-1)L+1)-Va(nL) to multiplexer 22_n.

The adjustment resistor string 21 delivers voltages Va(1)-Va(L) to multiplexer 25_1, voltage Va(L+1)-Va(2L) to multiplexer 25_2, $\cdots$, and voltages Va(((m/2)-1)L+1)-Va((m/2)L) to multiplexer $25_{m/2}$.

The resistor string 21 delivers voltages Va(((n-(m/2))L)+1)-Va(((n-(m/2)+1)L)) to multiplexer $25_{m/2+1}$, voltages Va ((n-(m/2)+1)L+1)-Va ((n-(m/2)+2)L) to multiplexer $25_{m/2+2}$, $\cdots$, and voltages Va((n-1)L+1)-Va(nL) to multiplexer 25_m.

The data latches 20_1-20_n and 23_1-23_m receive respective voltage address signal 105, which specifies the addresses of the γ-voltage or Vcom voltage for each of the data latches. γ-clock signals 11_1-11_n and COM clock signals 12_1-12_m rise in synchrony with the voltage address signal 105.

The data latch 20_1 latches the corresponding γ-voltage address in synchrony with the γ-clock signal 111 to deliver the latched address to the decoder 21_1. Similarly, the data latch 20_n latches the corresponding γ-voltage address in synchrony with the γ-clock signal 11n to deliver the latched address to the decoder 21_n. The γ-voltage address is set at an arbitrary number between zero and L during an initial adjustment, depending on the optical transmittance of the LCD panel.

The data latch 23_1 latches the corresponding Vcom-voltage address in synchrony with the COM clock signal 121, and delivers the latched address to the decoder 24_1. Similarly, the data latch 23_n latches the corresponding Vcom-voltage address in synchrony with the COM clock signal 12n, and delivers the latched address to the decoder 24_n. The Vcom-voltage address is set at an arbitrary number between zero and L during the initial adjustment, depending on the optical transmittance of the LCD panel.

The decoders 21_1-21_n decode the γ-voltage address to output a γ-voltage digital signals to the multiplexers 22_1-22_n. The decoders 24_1-24_n decode the Vcom-voltage address to output Vcom-voltage digital signals to the multiplexer 25_1-25_n. Each of the multiplexers 22_1-22_n and 25_1-25_n selects one of the corresponding voltage levels Va based on the input digital voltage signal.

More specifically, the multiplexer 22_1 selects one of the voltages Va(1)-Va(L) based on the γ-voltage digital signal, delivering an analog voltage Vb(1) corresponding to the selected voltage. The multiplexer 22_2 selects one of the voltages Va(L+1)-Va(2L) based on the γ-voltage digital signal, delivering an analog voltage Vb(2) corresponding to the selected voltage. Similarly, The multiplexer 22_n selects one of the voltages Va((n-1)L)-Va(nL) based on the γ-voltage digital signal, delivering an analog voltage Vb(n) corresponding to the selected voltage.

The multiplexer 25_1 selects one of the voltages Va(1)-Va(L)

based on the Vcom-voltage digital signal, delivering an analog voltage Vc(1) corresponding to the selected voltage. The multiplexer 25_2 selects one of the voltages Va(L+1)-Va(2L) based on the Vcom-voltage digital signal, delivering an analog voltage Vc(2) corresponding to the selected voltage. Similarly, the multiplexer $25_{m/2}$ selects one of the voltages Va(((m/2)-1)L)+1)-Va((m/2)L) based on the Vcom-voltage digital signal, delivering an analog voltage Vc(m/2) corresponding to the selected voltage.

The multiplexer $25_{m/2+1}$ selects one of the voltages Va((n-(m/2))L+1)-Va((n-(m/2)+1)L) based on the Vcom-voltage digital signal, delivering an analog voltage Vc((m/2)+1) corresponding to the selected voltage. The multiplexer $25_{m/2+2}$ selects one of the voltages Va(((n-(m/2)+1)L)+1)-Va((n-(m/2)+2)L) based on the Vcom-voltage digital signal, delivering an analog voltage Vc(m/2+2) corresponding to the selected voltage. Similarly, The multiplexer 25_m selects one of the voltages Va((n-1)L+1)-Va(nL) based on the Vcom-voltage digital signal, delivering an analog voltage Vc(m) corresponding to the selected voltage.

Each decoder and a corresponding multiplexer function as a DC converter, which receives a digital voltage signal specifying a specific voltage to thereby output an analog voltage signal having a value specified by the digital voltage signal

Referring to Fig. 4, the impedance converter 30 includes a γ -voltage operational amplifier block 31, a Vcom-voltage operational amplifier block 32, a capacitor block 33, and a switch

block 34. The γ-voltage operational amplifier block 31 includes n operational amplifiers A11-A1n each receiving a corresponding one of the γ-voltages Vb(1)-Vb(n). The Vcom-voltage operational amplifier block 32 includes m operational amplifiers A21-A2m each receiving a corresponding one of the Vcom voltages Vc(1)-Vc(m). Each operational amplifier operates as a voltage follower for impedance conversion, and delivers an output voltage corresponding to the input voltage.

The switch block 34 includes a first switch group including n switches S11a-S11na, a second switch group including n switches S11b-S1nb, and a third switch group including m switches S21-S2m, each of the switches being controlled by a polarity control signal 106 for effecting the AC driving scheme.

The capacitor block 33 includes (n+m) capacitors each shown by a node N11-N1n and N21-N2m in the drawing. Each capacitor is associated with a corresponding operational amplifier, absorbing the fluctuation of the potential at the output node of the corresponding operational amplifier.

Operational amplifier A11 receives a γ-voltage Vb(1), and delivers the same after the impedance conversion thereof through switch S11a or S11b as a γ-correction voltage Vd(1) or Vd(2). Operational amplifier A12 receives a γ-voltage, and delivers the same after the impedance conversion through switch S12a or S12b as the γ-correction voltage Vd(1) or Vd(2). Similarly, operational amplifier A1n receives a γ-voltage Vb(n), and

delivers the same after the impedance conversion through switch S1na or S1nb as the γ-correction voltage Vd(1) or Vd(2).

Operational amplifier A21 receives a Vcom voltage Vc(1) and delivers the same after the impedance conversion through switch S21 as the Vcom-correction voltage Ve. Operational amplifier A22 receives a Vcom voltage Vc(2) and delivers the same after the impedance conversion through switch S22 as the Vcom-correction voltage Ve. Similarly, operational amplifier A2n receives a Vcom voltage Vc(n) and delivers the same after the impedance conversion through switch S2n as the Vcom-correction voltage Ve.

The switch block 34 receives the polarity control signal 106, which specifies to close one of the switches in each of the switch groups, with the other switches being open in the each of the switch groups.

Referring to Fig. 5, the LCD driver 40 includes a γ-correction resistor string 41 and a display data output block 42. The γ-correction resistor string 41 includes (P-1) resistors Rb_1-Rb_P connected in series, which have specified resistances for approximating the optical transmittance profile, or γ-profile, of the LC layer as a whole. The γ-correction voltages Vd(1) and Vd(2) are supplied at both the ends of the γ-correction resistor string 41.

The γ-correction resistor string 41 divides the voltage between the voltage Vd(1) and the voltage Vd(2) to output the

divided voltages Vf(1)-Vf(P) to the display data output block 42.

The display data output block 42 includes J output sections each including a data latch 40_1-40_J, a decoder 41_1-41_J, a multiplexer 42_1-42_J and an operational amplifier 43_1-43_J. The functions of each output block except for the operational amplifier 43_1-43_J is similar to the γ-voltage generator section or the Vcom-voltage generator section of the voltage generator block 20. The number J corresponds, for example, the number of columns of the pixels on the screen of the LCD panel. That is, each display data output section delivers the output signal to a corresponding data line of the LCD panel.

Each display data output section receives a data signal 107, and selects one of the voltages Vf(1)-Vf(P) on the taps of the γ-correction resistor string 41 independently of the other display data output sections.

The number (P) of the output voltages of the γ-correction resistor string 41 corresponds to the number of gray-scale levels designed for the LCD panel 60.

Back to Fig. 2, the output signals of the LCD driver 40 are applied to data electrodes (not shown) of the LCD panel through the data lines, whereas the Vcom voltage selected by the impedance converter 30 is applied to the common electrode (not shown) of the LCD panel 60.

Upon power-on of the LCD control unit of the present embodiment, the γ-correction voltage signals 103 and the Vcom-

voltage signal 104 to be supplied to the LCD driver 40 and the LCD panel 60, respectively, are specified by the voltage address signal 105 of the signal controller 50 for adjustment of the LCD device. The signal controller 50 is controlled by a software and writes specified data in the register installed therein. The specified data stored in the LCD device is changed when the LCD panel 60 is first installed or replaced in the LCD device.

Now, the adjustment for the LCD device will be described. It is assumed that the number n of the output voltages from the γ -voltage generator block 22, the number m of the output voltages from the Vcom-voltage generator block 21, the number X=nL of taps of the adjustment resistor string 21, and the number P of the gray scale levels of the LCD panel 60 are 4, 2, 256 and 64, respectively.

The software for the signal controller 50 specifies the settings of the γ -correction voltages and the Vcom-voltage on the voltage address signal 105, and controls the AC driving scheme by the polarity control signal 106.

The γ -voltage addresses in the voltage address signal 105 of the high-potential voltage and the low-potential voltage during a positive-polarity drive are set at 1 and 2, respectively. The γ -voltage addresses of the high-potential voltage and the low-potential voltage during a negative-polarity drive are set at 1 and 2, respectively. The Vcom-voltage address in the voltage address signal 105 is set at 3 during both the positive- and negative-

polarity drive.

The polarity control signal 106 specifies based on the settings that switches S11a, S13b and S21 be selected during a positive-polarity drive and that switches S12a, S14b and S2m be selected during a negative-polarity drive.

The adjustment resistor string 21 generates 256 voltages Va(1)-Va(256), which are received by the γ-voltage generator block 22. The Vcom-voltage generator block 22 receives voltages Va(1)-Va(64) and voltages Va(193)-Va(256).

The multiplexer 221 selects Va(1) among the voltages Va(1)-Va(64) based on the voltage address signal 105, and delivers a voltage Vb(1) corresponding to Va(1). The multiplexer 222 selects Va(65) among the voltage Va(65)-Va(128), and delivers a voltage Vb(2) corresponding to Va(65). The multiplexer 223 selects Va(130) among the voltages Va(129)-Va(192) based on the voltage address signal 105, and delivers a voltage Vb(3) corresponding to Va(130). The multiplexer 224 selects Va(194) among the voltages Va(193)-Va(256) based on the voltage address signal 105, and delivers a voltage Vb(4) corresponding to Va(194).

The multiplexer 251 selects Va(3) among the voltages Va(1)-Va(64) based on the voltage address signal 105, and delivers a voltage Vc(1) corresponding to Va(3). The multiplexer 252 selects Va(195) among the voltage Va(193)-Va(256), and delivers a Vcom-correction voltage Vc(2) corresponding to

Va(195).

The impedance converter 30 receives the voltages Vb(1)-Vb(4), and selects voltages Vb(1) and Vb(3) or voltages Vb(4) and Vb(2) to output γ-correction voltages Vd(1) and Vd(2) corresponding to Va(1) and Va(130) or Va(194) and Va(65), respectively. The impedance converter 30 also receives voltages Vc(1) and Vc(2) and selects voltage Vc(1) or Vc(2) to output a Vcom voltage Ve corresponding to Va(3) or Va(195).

That is, if the γ-correction voltages of first and third groups are selected, the Vcom voltage of the fourth group is selected. On the other hand, if the γ-correction voltages of the second and fourth groups are selected, the Vcom voltage of the first group is selected.

The γ-correction resistor string 41 divides the voltage between Vd(1) and Vd(2) into 64 sections to output voltages Vf(1)-Vf(64) at the taps thereof. Each of the J display data output sections in the display data output block 42 independently selects one of the voltages Vf(1)-Vf(64) based on the data signal received from outside the LCD device, to thereby output a display data signal 108 having 64-gray-scale levels.

During a positive-polarity drive, each display voltage Vg of the display data signal 108 assumes a maximum of Vf(1)=Vd(1)=Vb(1)=Va(1) and a minimum of Vf(64)=Vd(2)=Vb(3)=Va(130), whereas the Vcom voltage Ve assumes a maximum of Ve=Vc(1)=Va(195).

During a negative-polarity drive, each display voltage Vg of the display data signal 108 assumes a maximum of Vf(1)=Vd(1)=Vb(2)=Va(65) and a minimum of Vf(64)=Vd(2)=Vb(4)=Va(194), whereas the Vcom voltage Ve assumes a maximum of Ve=Vc(2)=Va(3).

In the LCD control unit of the present embodiment, the voltage address signal 105 and the polarity control signal 106, which are supplied from the signal controller 50 based on a software, control the γ-correction voltages and the Vcom voltage, whereby the γ-correction voltages and the Vcom voltage can be adjusted by the software without using a hardware work such as addition of external resistors in the initial adjustment. In addition, the LCD control unit fabricated as a one-chip IC can be mounted on the LCD panel instead of the conventional LCD driver, whereby the number of members for the LCD device can be reduced to achieve smaller dimensions and lower costs of the LCD device.

In the exemplified configuration of the above embodiment, the γ-correction voltages included Vd(1) and Vd(2). However, the γ-correction voltages may include three or more voltages, which are applied to one or more tap of the γ-correction resistor string 41 in addition to both the ends thereof. In such a case, for example, voltages Vd(1), Vd(2) and Vd(3) may correspond to Vf(1), Vf(L/2) and vf(L), respectively. By using such a configuration, the adjustment of a higher voltage side and a lower

voltage side can be separately conducted to improve the accuracy of the adjustment of the γ-correction voltage to the γ-profile or optical transmittance of the LCD panel.

Since the above embodiment is described only for an example, the present invention is not limited to the above embodiment and various modifications or alterations can be easily made therefrom by those skilled in the art without departing from the scope of the present invention.